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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,533	12/30/2003	Chang-Youn Hwang	00939H-087700US	8876

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TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,533	HWANG ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Acknowledgment is made of applicant's amendment filed on Feb. 06, 2006. Therefore claims 1 and 11 as amended by the amendment and claims 2-10 and 12-20 are previously recited are currently pending in the Application.

Information Disclosure Statement

No further IDS have been filed after the IDS filed of January 27, 2004 .

Claim Rejections - 35 USC § 103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. ~~102~~ 103 that form the basis for the rejections under this section made in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 11 are rejected under 35 U.S.C. ~~102~~ 103(a) unpatentable over (b) as being ~~anticipated by~~ Tanaka (U. S. Patent No. 6,369,446, herein after Tanaka) previously applied and in view of Park et al. (USP No. 6,511,919, herein after Park) .

With respect to claims 1 and 11 Tanaka describes a method for forming a storage node of a semiconductor device, comprising the steps of: forming a plurality of bit line patterns (that defines a space there between- cl. 11) , each (bit line patterm –cl. 11) including a wire and a hard mask sequentially stacked over a surface of a substrate structure; (Tanaka figure 6A , wire 3 , hard mask – nitride layer 5 , similar to

Applicants' hard mask 40 in figure 3 etc. specification page 10-col. 13 lines 45-55) sequentially forming a first barrier layer and a first inter-layer insulation layer along a profile containing the (first and second) bit line patterns and filling first spaces between the bit line patterns; the first insulation layer being provided over the first barrier layer (Tanaka figure 6B # 24,2 5) .

Tanaka describes etching without specifically mentioning the presently newly added limitation without exposing the first barrier layer so that .

However Park, a patent from the same filed of endeavor describes in 5B etc. and col. 6 lines 17 to 39 describes etching the first inter-layer insulation layer (until a second space is defined between the first and second bit line patterns-cl. 11 Tanaka figures) without exposing the first barrier layer (provided between the first and second bit line patterns- cl. 11) so that a partial portion of the first inter-layer insulation layer remains on each space between the bit line patterns to form an etch stop layer and form precise self aligned contacts .

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Park's step of etching the first inter-layer insulation layer without exposing the first barrier layer so that a partial portion of the first inter-layer insulation layer remains on each space between the bit line patterns in Tanaka's method . The motivation to make above substition is to form an etch stop layer and form form precise self aligned contacts . (Park col.6 lines 25-27).

The remaining limitations of claims are :

(d) forming a second barrier layer over the first inter-layer insulation layer and the first barrier layer (and in to the second space) ; (Tanaka fig. 6 C #25) and (e) etching the first and the second barrier layers and the partial portion of the first inter-layer insulation layer to expose a surface of the substrate structure disposed between the (first and second- cl. 11) line patterns.,(the surface being provided directly below the second space- cl.11) (Tanaka fig. 6 C).

B. Claims 2-10, 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (U. S. Patent No. 6,369,446, herein after Tanaka) and Park et al. (USP No. 6,511,919, herein after Park) (as applied to claim 1 above and further in view of Huang (U.S. Patent No. 6,800,452, Huang). .

With respect to claim 2 Tanaka describes the method as recited in claim 1, further comprising the steps of performing a wet cleaning/etching process with use of the first barrier layer as an etch barrier layer after the step of (c) .

With respect to claims 2 and 12Tanaka describes the method as recited in claim, however Tanaka and Park do not specifically describe the step of wet cleaning.

However Huang, a patent from the same filed of endeavor describes in col.3 lines 55-60, etc. describes a wet cleaning process to remove an excess material remaining and thereby form a sufficient opening area in the trench and form wider spacers.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include Huang's wet cleaning process step in Tanaka's process to

remove an excess material remaining and thereby form a sufficient opening area in the trench and form wider spacers. (Huang col. 2 lines 10-15) .

With respect to claims 3 and 13 Tanaka describes the method as recited in claim 1,wherein the step includes the steps of (c-l) forming a storage node contact mask on the second inter-layer insulation layer; (Tanaka figure 42 (c) , col. 2 lines 55-60)and (c-2) performing a partial SAC etching process to the second inter-layer insulation layer with use of the storage node contact mask as an etch mask. (Huang col. 1 line 50-55)

With respect to claims 4 and 14 Tanaka describes the method as recited in claim 3 describes wherein the partial SAC etching process is carried out at a pressure of about 15 m torr to about 50 m torr with a supplied power range from about 1000 W to about 2000 W and employs an etch gas obtained by combining such gas as C4Fa , CsFa, C4F6, CHZFZ, Ar, CO and Na . (Huang col. 7 lines 1-5) .

With respect to claims 5 and 15 Tanaka describes the method as recited in claim 1, wherein the first barrier layer is formed by employing a low pressure technique and the second barrier layer is formed by employing a plasma deposition technique. (Haung col. 2 lines 55-60)

With respect to claims 6 and 16 Tanaka describes the method as recited in claim 5, wherein the second barrier layer is a nitride layer and the nitride layer is deposited with a thickness ranging from about 500 to about 2000 at a temperature in a range from about 500 OC to about by using a source gas of silane (SiH4) and ammonia (NH_3). (Haung col. 2 line 60-65, claims 13, 23).

With respect to claims 7 and 17 Tanaka describes the method as recited in claim 1, wherein the etch-back process employed for etching the second barrier layer is carried out at a pressure of about 15 mtorr to about 50 mtorr with a supplied power in a range from about 1000 W to about 2000 W and employs an etch gas obtained by combining such gas as C4F8 , CsFa , C4F6 , CHZF; , Ar , 0: , CO and N2 . (see rejection of claim 4 above and Tanaka col.11 examples 5-9, etc. Haung claims 13, 23).

With respect to claims 8 and 18 Tanaka describes the method as recited in claim wherein the substrate structure includes a plurality of plugs formed on a substrate and a second inter-layer insulation layer. (Tanaka figure 20 A etc. Haung figure 13 etc.).

With respect to claims 9 and 19 Tanaka describes the method as barrier layer is more and corners of each bit recited in claim 1, wherein the second barrier layer is more thickly deposited on an upper surface line pattern than at sidewalls of each bit line pattern. (Tanaka figure 16c, Haung figure 5).

With respect to claims 10 and 20 Tanaka describes the method as recited in claim 1, wherein at the step (e) of etching the first and the second barrier layers and the remaining first inter-layer insulation layer, a spacer is simultaneously formed with the first inter-layer insulation layer at the sidewalls of each bit line pattern. (Haung figure 5).

Applicant's arguments with respect to claim 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571)272-1718. The examiner can normally be reached on 8.00 to 5.00.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven H. Rao

Patent Examiner

September 13, 2005.

...DNG CHAM
...MARY EXAMINER